ABSTRACT

The present invention provides a unique methodology for device and process technology that results in significant improvements in the parameters of the active devices of all integrated technologies including: bipolar, CMOS, BiCmos, BCD (Bipolar, Cmos, DMOS), and DMOS. The approach results in fewer process steps than the standard approach in each of these technologies, while providing lower capacitance, higher speed, lower power dissipation, lower Ron, lower ground resistance, lower output resistance, reduced de-biasing at high current, higher breakdown voltage, higher beta and over a broader current range while providing significant reduction in die size. Use of this approach also results in improved Schottky diodes and solar cells.

For most integrated circuits, this approach results in the elimination of the two longest time and highest temperature diffusion steps (isolation and sinker), along with their masking steps. This results in a lower overall temperature budget for the total process, allowing for improved control of related parameters. For bipolar devices, it provides an emitter with lower emitter de-biasing, which is important in high-current devices.

Similar advantages are obtained on the parameters of the other technologies indicated. This monolithic approach incorporates a unique slot process and slot location to provide a buried power buss (BPB), which results in metal thicknesses that are 5 to 10 times the normal thickness and provides circuit functions that are equivalent to triple metal technology, while only requiring the patterning of a single thin metal.